ing over 100 mW from 2–6.2 GHz and 5.9–12.4 GHz, respectively, with good match and ample gain.

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Wide-Band Gallium Arsenide Power MESFET Amplifiers

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Abstract—**The performance, with emphasis on wide bandwidth, that can be expected of linear medium power GaAs microwave MESFET (metal semiconductor field-effect-transistor) amplifiers is discussed. It starts with measured scattering parameters of devices and proceeds through computer-optimized device modeling, to amplifier circuit designs and performance results. It shows computed and measured octave bandwidth performance and reveals that decade bandwidth is feasible. It discusses single-ended and balanced amplifier design approaches. Some practical designs with performance results are presented, with circuit topologies which are easily realizable in microstrip.**

I. INTRODUCTION

MICROWAVE power MESFET's capable of approximately 1-W output power in the 4–9-GHz frequency range have been announced [1]–[3]. These results indicate significant progress in power FET technology leading to commercial availability in the near future. The Naval Research Laboratory has performed circuit computations and experimental amplifier construction using medium power, single-, and two-cell devices similar to those described in [3]. This paper reports the results of the investigation.

Section II gives general characteristics and modeling information on the devices used. Section III discusses the theoretical and practical bandwidth capability of devices and amplifiers. Section IV presents experimental results for single-ended and balanced amplifiers.

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II. GENERAL DEVICE CHARACTERISTICS

The configuration of the power MESFET flip-chip carrier is illustrated in Fig. 1. The chip's raised source pads are bonded to a pedestal formed as part of the carrier providing RF ground and heat sinking. The gate and drain connections are made with pairs (only one shown) of 0.0025-cm-diam bond wires to the metallized alumina standoff chips on both sides of the transistor chip. Additional cells may be

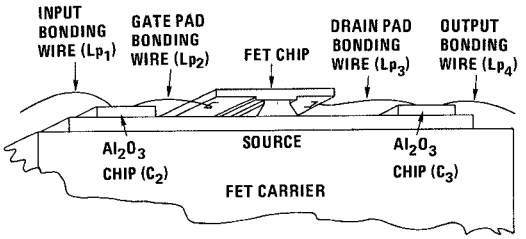


Fig. 1. Power MESFET flip-chip configuration.

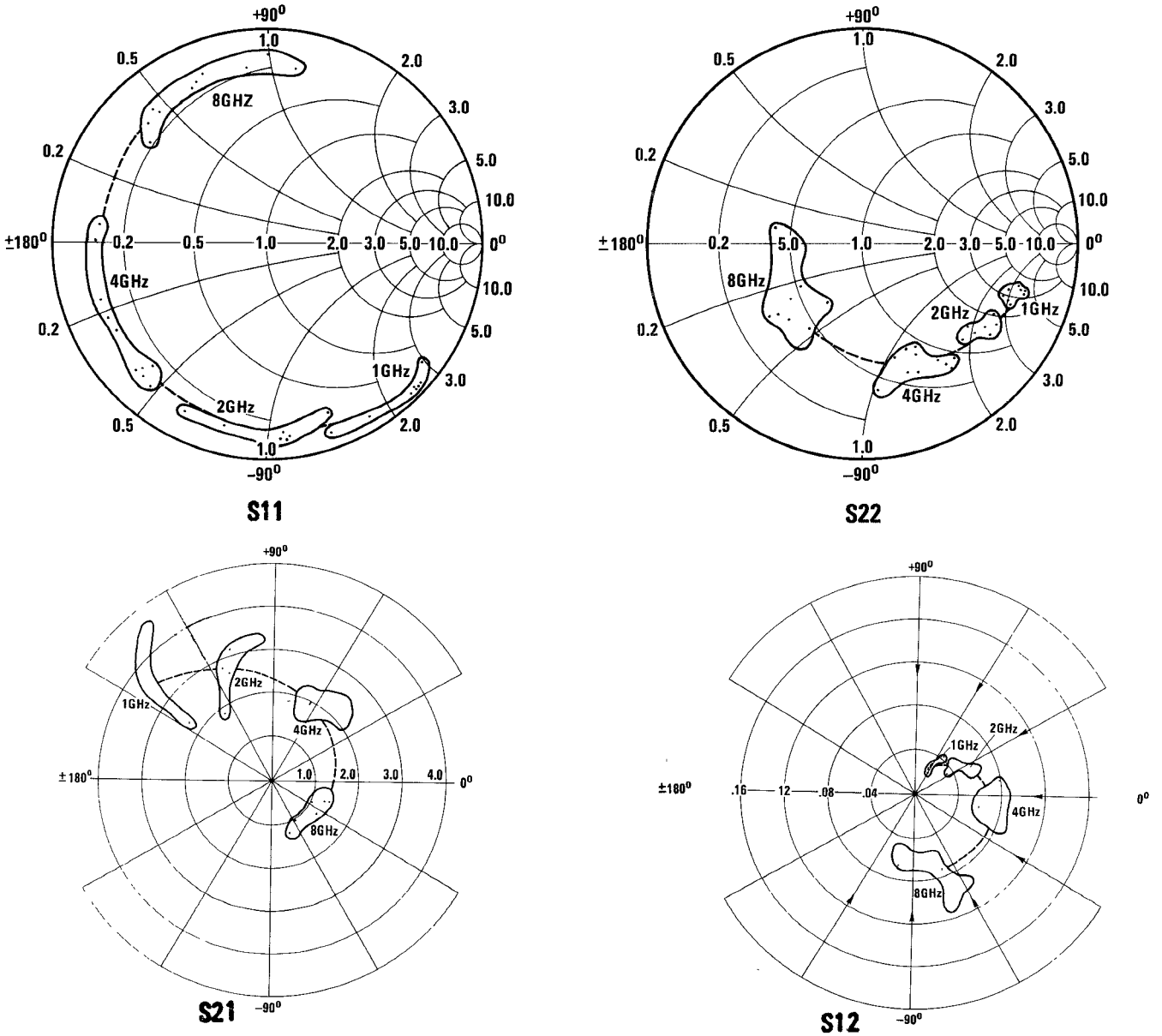
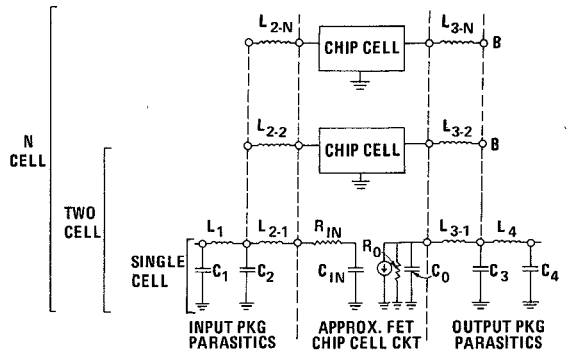


Fig. 2. Range of measured S-parameter values, single-cell "packaged" devices.

added by interconnecting respective cell pads to the alumina standoff.

Small-signal S-parameter characterization was performed with the input and output reference planes defined as the points at which the input and output bond wires attach to the external circuitry. The physical spacing between these two planes is approximately 0.24 cm. The range of values of the S parameters obtained for several single-cell devices is shown in Fig. 2. The output power at 1-dB gain compression at 8 GHz was also measured. These values ranged



	C_1 pf	L_1 nh	C_2 pf	L_2 nh	R_{IN} Ω	C_{IN} pf	gm mmho	R_0 Ω	C_0 pf	L_3 nh	C_3 pf	L_4 nh	C_4 pf
SINGLE-CELL	13	65	16	31	6.1	15	55	348	.13	.42	14	145	.20
TWO-CELL	.06	.46	.18	.17	4.8	1.3	100	220	.20	41	.22	40	.21
				.17	4.8	1.3	100	220	.20	41			

Fig. 3. Approximate equivalent circuit of typical power MESFET's.

from about 90 to 250 mW for ten units, averaging 150 mW. The devices were typically unconditionally stable above 4 GHz and the source and load impedances which could produce oscillations below 4 GHz were avoidable.

An approximate equivalent circuit for the transistor and its "parasitic" input and output elements is shown in Fig. 3. The package parasitics are represented by the bond lead inductances L_1, L_2, L_3, and L_4. The standoff chip capacitances and the circuit interface fringing capacitances are shown as C_1, C_2, C_3, and C_4. The circuit for a single cell on the MESFET chip can be approximated by an input series network R_{in} and C_{IN}, and an output network consisting of a current generator and the parallel shunt components R_O and C_O. The isolation between the input and output equivalent circuit networks (reverse transmission parameter S_{12}) is sufficiently high to neglect the associated feedback elements. Utilizing a computer-aided design optimization program, the values of the equivalent circuit parameters were derived. The element values were optimized to fit the measured input and output S parameters S_{11} and S_{22}. The value of the transconductance was optimized to fit the forward transmission gain S_{21}. The computed parameters are given in Fig. 3. The values of the parasitic elements compare favorably with those which can be calculated from their physical dimensions.

III. Circuit Considerations and Amplifier Performance Calculations

This section gives a variety of computations on the MESFET devices and amplifier circuits. Section III-A gives information related to 4–8-GHz octave bandwidth applications, using single-cell devices. Section III-B discusses the theoretical performance capability of a two-cell device, also for the 4–8-GHz octave band. Section III-C presents computed amplifier performance using a single-cell transistor in the 2–4-GHz octave band. Section III-D gives information for 1–10-GHz decade bandwidth operation. Section III-E discusses a design approach for matched single-ended amplifiers.

A. Octave Band (4–8 GHz)

Theoretical Performance Limit—Chip without External Parasitics: The fundamental theoretical limitations on the broad-band operation of amplifiers are dependent on the reactive constraints of the device parameters. The gain-bandwidth restrictions can be determined from the relationships of Bode [4] and Fano [5], and are related to the device Q's. Approximate equivalent circuits for single-cell and multi-cell power MESFET devices have been shown in Fig. 3. Consider, for example, a single-cell chip with no parasitic elements, operating over the 4–8-GHz frequency range. The input and output chip Q's at 6 GHz are approximately 2.9 and 1.7, respectively. The exactness of match given by the minimum attainable flat reflection coefficient over a given band is inversely related to the device Q. The chip input circuit has the higher Q and thereby primarily limits the attainable amplifier bandwidth. By matching to the chip's input circuit over the 4–8-GHz octave band, a minimum flat reflection coefficient of 0.2 can be theoretically obtained. The corresponding input transmission loss is about 0.2 dB. Similarly, a flat output reflection coefficient of 0.063 is theoretically attainable, with an associated transmission loss of 0.02 dB. Therefore an octave band (4–8-GHz) single-cell power MESFET amplifier can be designed having a theoretical gain response which is 0.22 dB less than the inherent conjugately matched gain response, GMAX, of the transistor chip. For all devices investigated, the inherent matched gain rolls off at 6 dB per octave over the full 1–10-GHz frequency range. The response of the aforementioned "flat-matched" amplifier would have a gain slope of 6 dB per octave. Gain tapering in the input or output networks, or both, must be employed to obtain flat response.

A discussion of reactive gain tapering is given by Ku and Peterson [6]. In their work expressions are developed for the gain-bandwidth limitations of gain-tapered matching networks into high- and low-pass load configurations like the power MESFET input and output circuits. From [6, expression 31 or related graphs] it can be determined that the minimum allowable normalized input time constant τ_N is approximately 0.14 to be able to generate a network having zero loss at 8 GHz and a 6 dB per octave low-frequency rolloff. The term τ_N is defined as $\tau_N = \omega_H \tau$, where ω_H is the radian frequency value at the upper band edge and τ is the product of the MESFET chip input resistance and capacitance. The value of τ_N at 8 GHz for the single-cell power MESFET chip is 0.46; thus such an input network is possible. Employing the idealized gain-tapered input matching circuit and flat output matching network, an overall flat amplifier gain response can be realized. The value of gain would be 0.02 dB less than the 8-GHz value of GMAX. Alternately, if desired the gain tapering could be done in the output network with the input flat matched. Employing [6, fig. 9], the resultant overall flat amplifier gain response would be 0.2 dB below the 8-GHz value of GMAX.

Theoretical Performance Limit—Chip with External Parasitics: In the following discussion the parasitic elements of the chip's input and output connections (described in Fig. 3) are treated as part of the transistor. A slightly dif-

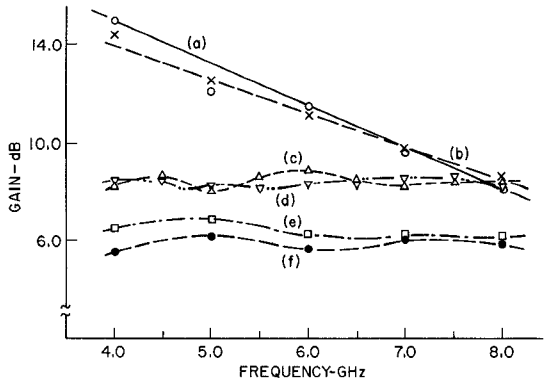


Fig. 4. Computed and measured performance responses of a single-cell power MESFET. (a) Max. unilateral gain calculated from measured S parameters. (b) Max. unilateral gain calculated from equivalent circuit parameters. (c) Calculated amplifier gain using lumped elements. (d) Calculated amplifier gain using distributed elements. (e) Calculated amplifier gain using easily realizable elements in microstrip. (f) Measured amplifier gain using circuit topology of (e). See Section III-A of text.

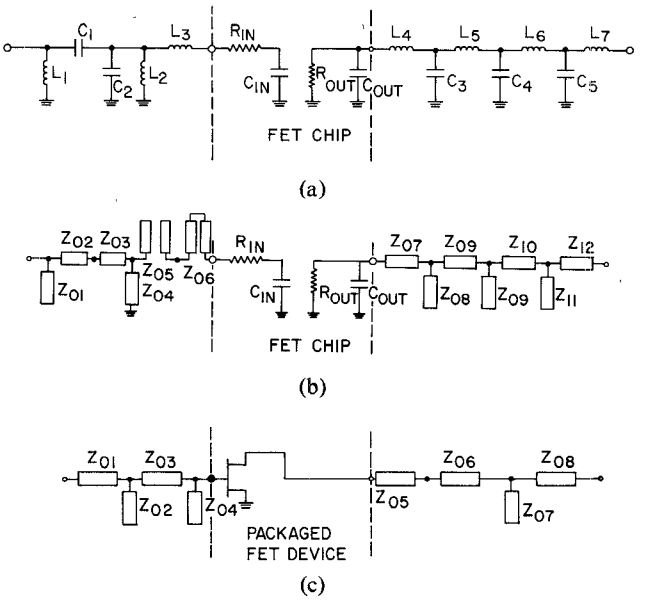


Fig. 5. Power MESFET matching network topologies. (a) Lumped. Produced computed curve (c) in Fig. 4. (b) Distributed. Produced computed curve (d) in Fig. 4. (c) Easily realizable microstrip. Produced computed curve (e) and measured curve (f) in Fig. 4.

ferent approach is necessary to arrive at suitable values for Q's. Inclusion of these elements increases the input and output Q's from the chip values. The higher values may be approximated from a Smith chart plot of the S_{11} and S_{22} parameters by calculating Q values from the expression

$$Q = \frac{f_0}{2} \frac{\Delta x/\Delta f}{R}$$

as described in [7, sec. 5], where $(\Delta x/\Delta f)$ is the reactance/frequency slope at center frequency f_0 and R is the input resistance at that frequency. An alternate numerical approach used in this paper to estimate the input and output circuit Q's was to compute the 3-dB bandwidth of transmission into the equivalent circuits preceded by a series element selected to resonate the circuit at f_0, the frequency at which Q was to be determined. The source impedance of the driving signal was made approximately zero so that $Q = f_0/$ 3-dB bandwidth yielded the unloaded circuit Q at f_0. The Q values obtained by the two methods were in agreement. For the case being considered, input and output Q's of approximately 5.5 and 3.3, respectively, result for the single-cell device. Flat output matching to a reflection coefficient of 0.24 is theoretically possible. A tapered-gain input network having zero loss at 8 GHz and 6 dB per octave slope is also theoretically possible. Thus a flat amplifier gain at approximately 0.25 dB below the 8-GHz value of GMAX is obtainable.

Theoretical Circuit Calculations: The curves shown in Fig. 4 illustrate some typical computed and measured performance results on a single-cell power MESFET in the 4–8-GHz band. Curve (a) of Fig. 4 gives the maximum unilateral gain of the transistor, defined as in [8], derived from measured S parameters which include the packaging parasitics. The 6 dB per octave downward gain slope of the transistor is apparent. Curve (b) of Fig. 4 is a plot of the equivalent maximum unilateral gain, derived directly from the equivalent single-cell circuit and parameter values given in Fig. 3. Curve (c) gives the computed response of an amplifier using lumped element input and output matching networks, using only the chip parameters to represent the transistor (no packaging parasitics between the chip and the matching networks). These circuits are shown in Fig. 5(a). The output side is flat matched and the starting element values before computer optimization were taken from Matthaei [9]. The input side is gain-taper matched and uses a configuration and preoptimization element values suggested by Peterson *et al.* [10]. The values of the chip elements were, of course, held constant during the circuit optimizations. Curve (d) of Fig. 4 gives the computed response of an amplifier using a design approach similar to the one which produced curve (c), but here the input and output networks are distributed. These network topologies are shown in Fig. 5(b). The flat matching output network is a distributed approximation of the preceding lumped network and the gain-tapered input network is suggested by Peterson *et al.* [10].

Practical Circuit Calculations: The preceding circuit information is useful in establishing theoretical limits of gain performance, but practical realizable networks must also be evaluated. A power MESFET amplifier stage was designed using input and output networks easily realizable in microstrip. The circuit topologies are shown in Fig. 5(c). The transistor used was similar to the one analyzed earlier with packaging parasitics. The external microstrip circuit elements were computer optimized for maximum flat gain. The predicted and measured gain responses of the amplifier are represented by curves (e) and (f) of Fig. 4. The measured response is that of the complete amplifier including the bias networks and dc blocks. The bias networks included miniature five-turn hand-wound coils, specially developed for this application. The dc blocks were chip capacitors. Further information on this amplifier is presented in Section IV.

Parasitic Optimization: The following computational exercise was carried out to examine the relative advantage of selecting a better set of transistor package parasitic elements. First the values of the package elements were

TABLE I
MEASURED S PARAMETERS AND CALCULATED MAXIMUM UNILATERAL GAIN (MUG) OF A TWO-CELL POWER MESFET

Freq. (GHz)	$\lvert S_{11}\rvert/\underline{\theta^\circ}$	$\lvert S_{21}\rvert/\underline{\theta^\circ}$	$\lvert S_{12}\rvert/\underline{\theta^\circ}$	$\lvert S_{22}\rvert/\underline{\theta^\circ}$	MUG (dB)
4.0	.881/-160	1.960/ 51	.042/ 7	.374/-108	13.0
4.5	.891/-166	1.757/ 43	.048/ -1	.507/-114	13.1
5.0	.889/-172	1.640/ 36	.054/-17	.636/-125	13.4
5.5	.854/ 179	1.474/ 27	.051/-35	.652/-136	11.4
6.0	.841/ 170	1.468/ 18	.048/-49	.618/-149	10.8
6.5	.828/ 157	1.417/ 7	.041/-60	.529/-157	9.5
7.0	.827/ 141	1.352/ -4	.034/-63	.438/-162	8.5
7.5	.820/ 127	1.207/-16	.033/-58	.404/-164	7.3
8.0	.834/ 121	1.074/-25	.032/-58	.396/-168	6.5
8.5	.900/ 116	1.013/-35	.034/-55	.438/-175	8.2
9.0	.943/ 113	.900/-47	.035/-53	.551/ 178	10.2
9.5	.954/ 111	.774/-59	.041/-55	.708/ 167	11.3
10.0	.943/ 112	.624/-64	.040/-60	.844/ 154	10.9
10.5	.904/ 113	.522/-67	.042/-56	.895/ 142	8.7
11.0	.872/ 117	.483/-68	.038/-53	.813/ 133	4.6
11.5	.841/ 119	.479/-66	.046/-43	.702/ 128	1.9
12.0	.794/ 120	.472/-69	.059/-44	.600/ 130	-0.2

Note: Drain voltage = +8.0 V, gate voltage = 0.0 V, and drain current = 360 mA. See text, Section III-B.

computer adjusted for improved match, with no external circuitry, over the 4–8-GHz band. Values of these adjusted elements are: $C_1 = 0.57$ pF, $L_1 = 0.20$ nH, $C_2 = 0.35$ pF, $L_2 = 0.80$ nH, $L_3 = 0.62$ nH, $C_3 = 0.12$ pF, $L_4 = 2.44$ nH, and $C_4 = 0.01$ pF. The external microstrip circuit elements were then optimized for gain, using the new computed S-parameter values for the transistor with optimized parasitics. The external circuit topology is that of Fig. 5(c). The computed response of this amplifier was approximately 1.5 dB higher over the band than with the original parasitics.

B. Two-Cell Device Calculations

A two-cell device, used to achieve higher power performance (0.3–0.4 W or so at 8 GHz), is illustrated schematically in Fig. 3. The additional cell is assumed to be connected in parallel, with inductors L_{2-2} and L_{3-2} representing the bond path. A specific device whose S parameters are given in Table I was analyzed in the 4–8-GHz frequency range. In a manner similar to that used for single-cell devices, the equivalent circuit parameters were determined by computer optimization to fit the measured S parameters. The input and output Q's at 6 GHz were calculated from the equivalent circuit parameters, including all the parasitic elements, to be approximately 9.2 and 2.5, respectively. An output port flat matching network is possible, producing about 0.1 dB of transmission loss. The value of τ_N for the two-cell transistor input is about 0.14; therefore a 6 dB per octave tapered input matching network with zero loss at 8 GHz is marginally possible. Thus an octave band (4–8-GHz) flat-gain amplifier is theoretically possible with the two-cell power MESFET, but parasitic element optimization might be necessary to realize the theoretical gain with realistic external networks. No further two-cell matching network computations were made.

C. Octave Band (2–4 GHz)

Calculations were made on typical one-cell transistor amplifier circuit topologies to operate in the 2–4-GHz octave band. Methods employed were similar to those described previously for the 4–8-GHz octave band. The maximum unilateral gain of the transistor at 4 GHz was 14 dB. To provide a reference point of theoretical gain achievable, an amplifier was designed with complex distributed matching networks and optimized parasitic elements. Approximately 14-dB computed flat gain resulted from 2 to 4 GHz. A practical design was also carried out with easily realizable matching networks for microstrip and with the actual parasitic elements. The external matching networks consisted of four sections of alternating series lines and shunt open stub lines on input and output. The resultant computed gain was 11.7 ± 0.5 dB from 2 to 4 GHz. Thus amplifiers using single-cell devices at the 0.1–0.3-W output power capability level can be readily designed for the 2–4-GHz octave band, having flat small-signal gain approximately 6 dB higher than for the 4–8-GHz octave band.

D. Decade Band (1–10 GHz)

Full decade bandwidth operation from 1 to 10 GHz has been considered. The first case looks at the theoretically achievable flat performance over the decade. Consider the single-cell chip, without parasitics, whose equivalent circuit and element values are given in Fig. 3. Theoretical minimum flat reflection coefficients of 0.548 and 0.358 can be realized at the input and output ports, respectively. The corresponding respective transmission losses are 1.55 and 0.60 dB. The normalized input time constant τ_N of the single-cell at 10 GHz is 0.57. From [6, expression 31 or the related curves in fig. 11] the minimum input time constant is 0.20 for an idealized network having 6 dB per octave slope and 0-dB transmission loss at the upper edge (10 GHz). Consequently, ideal networks at the chip ports can be formulated to provide a flat 1–10-GHz amplifier. The output network would produce a constant 0.6-dB reduction from GMAX and the input network would provide the 6 dB per octave slope with no gain loss at the upper end of the band. Typically, GMAX at 10 GHz is about 6 dB; therefore the theoretical flat gain response over the 1–10-GHz band is approximately 5.4 dB.

The second case considers a circuit design for the same single-cell chip, but including the parasitic elements given in Fig. 3. It is expected that considerably less than the theoretical maximum gain can actually be achieved for this case, due to the nonoptimum values of the parasitic elements. External input and output networks, each consisting of five impedance transforming series transmission lines, were formulated and optimized. Curve (a) of Fig. 6 plots this amplifier's computed gain performance.

The last case considers the use of the same external circuit

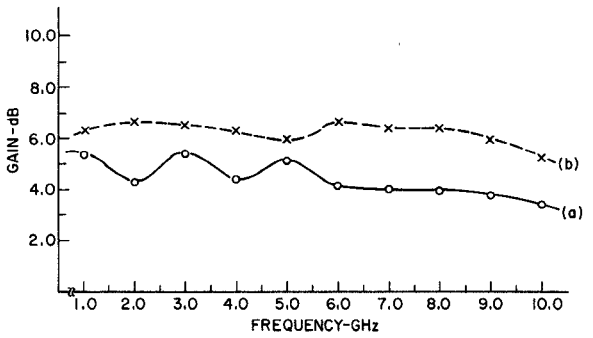


Fig. 6. Computed decade bandwidth (1–10-GHz) power MESFET amplifier responses.

TABLE II
MEASURED S PARAMETERS AND CALCULATED MUG OF A SINGLE-CELL MESFET

Freq. (GHz)	$\lvert S_{11}\rvert\angle\theta°$	$\lvert S_{21}\rvert\angle\theta°$	$\lvert S_{12}\rvert\angle\theta°$	$\lvert S_{22}\rvert\angle\theta°$	MUG (dB)
4.0	.82 /-135	2.194 /70	.085 /0	.535 /-62	13.1
5.0	.788 /-167	1.959 /47	.087 /-19	.524 /-70	11.5
6.0	.76 /162	1.673 /25	.083 /-36	.486 /-75	9.4
7.0	.773 /140	1.46 /5	.082 /-45	.405 /-89	8.0
8.0	.817 /131	1.298 /-11	.093 /-56	.314 /-120	7.5

Note: $V_D = +6.0$ V, $V_G = 0.0$ V, and $I_D = 120$ mA. See text Section IV-A.

topology as was used previously, but allows the parasitic elements to take on new optimized values for the decade band. The parasitic element adjustment was done to optimize S_{11} and S_{22} of the "packaged" transistor, independent of the external circuitry. The external circuitry was then re-optimized for the new values of parasitic elements. The resultant computed gain performance is given by curve (b) of Fig. 6. The result, using reasonable networks, shows a good approximation of the theoretical 5.4-dB flat gain over the 1–10-GHz decade.

E. Matched Single-Ended Amplifier with Flat Gain Response

For narrower bandwidths than have been so far discussed, reactively matched single-ended amplifier stages are possible. Low input and output VSWR's are achievable simultaneously over some bandwidth which is inversely proportional to the device input and output circuit Q's. One of the problems with this approach is the resultant amplifier gain slope of approximately 6 dB per octave. A way of overcoming the gain slope and increasing the bandwidth without greatly sacrificing overall gain is to include resistive loading in the amplifier input circuit.

Using this approach, a typical single-cell MESFET chip produced computed input and output VSWR's of less than 2.0 and gain of 6.6–7.7 dB over a 4.7–7.8-GHz band. The input circuit topology (not necessarily the optimum) included 50-Ω resistors to ground at the end of transmission line stubs.

IV. Experimental Amplifier Results

The matching networks for the experimental amplifiers to be discussed were designed from the measured small-signal S parameters of the power MESFET's. The transistors used were single-cell units with parasitic packaging elements similar to those given in Fig. 3. Circuit topologies were selected for fabrication simplicity in microstrip and were computer optimized for desired gain performance. Both designs were for the 4–8-GHz octave band but the matching network approaches were quite different.

A. Single Transistor Stages

High/Low Impedance Series Line Matching: The first experimental example used the transistor whose measured S parameters and calculated maximum unilateral gain are given in Table II. Series sections of alternating high- and low-impedance transmission line were selected as the matching network topology for this amplifier design. Interest in this topology is stimulated by the availability of an approximate model for large microstrip step discontinuities developed at the Naval Research Laboratory [11]. For additional simplicity all the high-impedance sections were made 50 Ω and all the low-impedance sections were made 10 Ω. The circuit configuration, the computed amplifier gain, and the measured gain are shown in Fig. 7. The amplifier was constructed with etched 50-Ω lines on 0.0635-cm-thick alumina and indium foil overlays to approximate the computer optimized dimensions for the low-impedance line sections. External bias insertion devices were used and the measured gain results do not include their losses. Two additional amplifiers were similarly constructed for balanced amplifier tests to be described in Section IV-B.

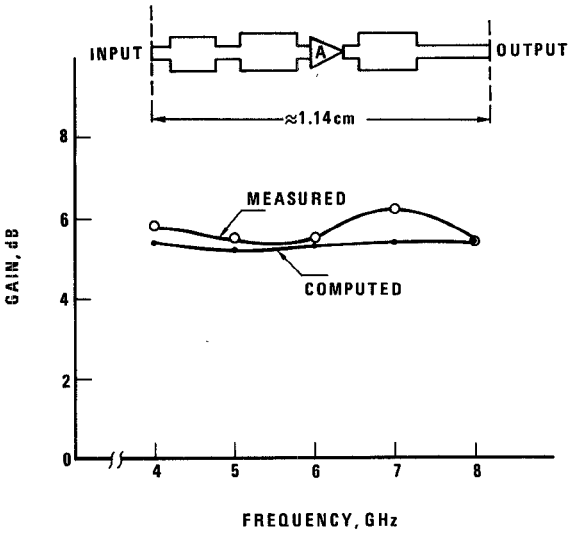


Fig. 7. Gain performance, amplifier with high/low-impedance series line matching.

Series Line/Shunt Stub Matching: In addition to the amplifiers using high- and low-impedance line section matching networks, another pair of completely integrated amplifiers was designed, fabricated, and tested. Bias and dc blocking networks are built in and all measurements include their losses. These amplifiers also used single-cell devices with parasitic elements similar to those shown in Fig. 3. Their measured S parameters and maximum unilateral gain values are listed in Table III, and the matching

TABLE III
MEASURED S PARAMETERS AND CALCULATED MUG OF SINGLE-CELL MESFET'S USED IN FULLY INTEGRATED AMPLIFIERS

Freq. (GHz)	Device in Amplifier A1 $\lvert S_{11}\rvert/\theta°$	$\lvert S_{21}\rvert/\theta°$	$\lvert S_{12}\rvert/\theta°$	$\lvert S_{22}\rvert/\theta°$	MUG dB	Device in Amplifier A2 $\lvert S_{11}\rvert/\theta°$	$\lvert S_{21}\rvert/\theta°$	$\lvert S_{12}\rvert/\theta°$	$\lvert S_{22}\rvert/\theta°$	MUG (dB)
1.0	.970/-46	3.232/144	.030/ 61	.784/-16	26.6	.968/ -42	3.423/145	.029/ 62	.715/-17	25.7
2.0	.886/-85	2.618/113	.045/ 35	.728/-31	18.3	.916/ -84	3.004/112	.048/ 34	.662/-38	20.0
3.0	.874/-113	2.379/ 90	.057/ 18	.709/-38	16.8	.858/-114	2.389/ 85	.055/ 9	.627/-57	15.5
4.0	.821/-155	1.988/ 59	.069/- 3	.681/-51	13.5	.845/-133	1.954/ 64	.060/-10	.631/-70	13.5
5.0	.821/-177	1.567/ 36	.064/-22	.615/-77	10.8	.786/-153	1.721/ 47	.057/-34	.649/-74	11.3
6.0	.815/ 172	1.383/ 18	.064/-28	.694/-88	10.4	.770/-177	1.647/ 28	.046/-51	.662/-76	10.7
7.0	.812/ 133	1.348/ -8	.075/-44	.750/-92	10.9	.835/ 151	1.402/ 6	.055/-51	.627/-91	10.3
8.0	.845/ 111	1.049/-27	.063/-70	.544/-121	7.4	.792/ 130	1.396/-19	.073/-69	.465/-122	8.2
9.0	.894/ 113	.899/-53	.055/-81	.694/-154	8.9	.774/ 113	1.217/-46	.079/-87	.501/-155	6.9
10.0	.734/ 106	.752/-67	.059/-92	.784/-162	5.0	.722/ 96	.961/-73	.085/-105	.673/-173	5.5
11.0	.810/ 59	.850/-91	.062/-113	.594/-169	5.1	.652/ 82	.673/-86	.074/-118	.746/-178	2.5
12.0	.851/ 45	.653/-127	.058/-139	.707/ 146	4.9	.635/ 77	.560/-91	.064/-119	.739/-177	0.6

Note: $V_{D1} = V_{D2} = +8.0$ V, $V_{G1} = V_{G2} = 0.0$ V, $I_{D1} = 185$ mA, and $I_{D2} = 235$ mA. See text, Section IV-A.

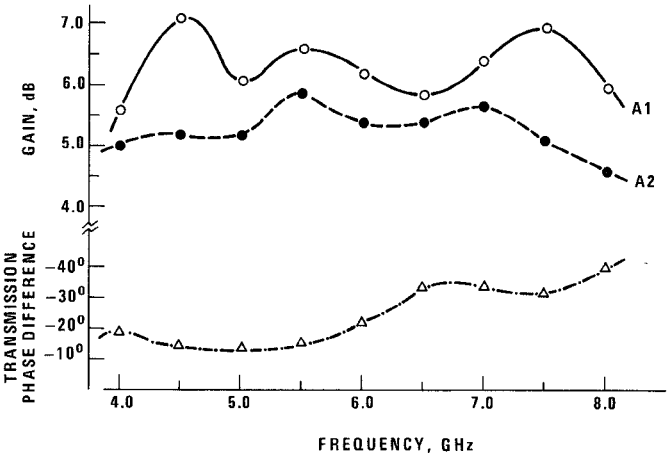


Fig. 8. Measured performance, two integrated MESFET amplifiers with series line/shunt stub matching.

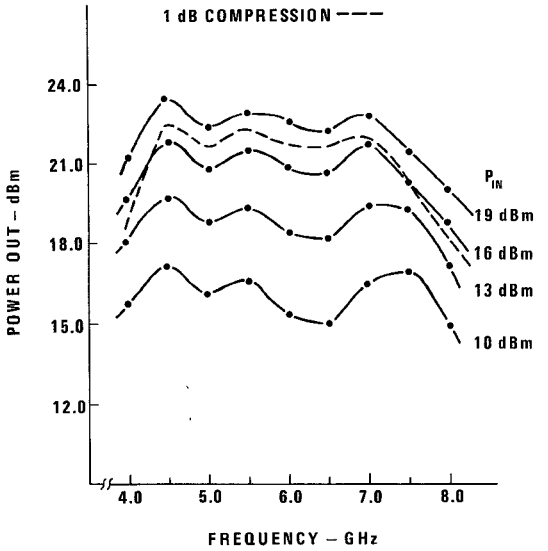


Fig. 9. Measured power response of an integrated MESFET amplifier (A1 of Fig. 8).

circuit topologies are illustrated in Fig. 5(c). The input and output matching networks were simultaneously optimized for gain flatness over the 4–8-GHz octave band. Microstrip circuits were constructed on 0.0635-cm-thick alumina, according to the computer optimization results. Initial testing of the amplifier stages showed a sharp rolloff in gain at 8 GHz, requiring trimming of the transmission line stubs to flatten the measured small-signal gain response. The final measured gain response curves are given in Fig. 8. Transmission phase difference between the two amplifiers is also shown in this figure and will be discussed in Section IV-B.

Output power measurements are given in Fig. 9 for amplifier number 1 of the pair. Output is shown over the full band for increasing values of input power, with the lowest curve being essentially the same as the small-signal curve. The approximate curve of the 1-dB gain compression point is shown dashed. It should be pointed out that the transistor used in amplifier number 1 demonstrated in earlier single frequency measurements an inherent output power capability of +24 dBm at 1-dB gain compression at 8 GHz. This had been measured with the bias conditions and the RF tuning simultaneously adjusted at that frequency for maximization of output power. Allowing for the losses of the bias and blocking networks (0.5–1.0 dB), this performance is being approached over most of the 4–8-GHz band, even though the circuits were selected for optimum wide-band small-signal gain.

Intermodulation distortion information on amplifier number 1 appears in Fig. 10 for operation at 6 GHz. The fundamental frequency curve is plotted there with the data points indicated. The two-tone method with a frequency difference of 10 MHz was used to measure third-order intermodulation levels (points A and B in Fig. 10). The intercept point (IP) occurs at +35 dBm or approximately 13.7 dB above the 1-dB compression level. For amplifier number 2, which employed a transistor of considerably lower inherent power capability, the intercept occurred at

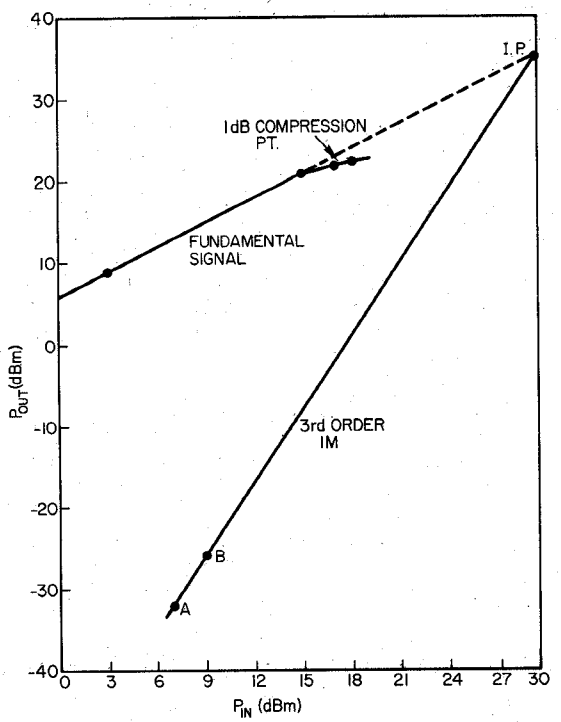


Fig. 10. Power response and intermodulation characteristics of an integrated MESFET amplifier at 6 GHz (Al of Fig. 8).

only +28 dBm which was about 8 dB above the 1-dB compression point. These two amplifiers, in spite of their dissimilarity, will be quadrature combined and further discussed in the following section.

B. Balanced Power Amplifiers

The input and output VSWR's of wide-band amplifiers with reactive gain flattening are unconstrained and large in contrast to the narrower band "matched" approach discussed briefly in Section III-E. Kurokawa [12] presented a thorough discussion of the theory and advantages of balanced transistor amplifier designs. For octave bandwidth amplifiers a single-section quadrature 3-dB directional coupler is suitable for the power divide/combine networks.

High/Low Impedance Series Line Matching: Two amplifiers were constructed having the transmission gain, phase differential, and input and output VSWR's shown in Fig. 11. The circuits are of high/low-impedance transmission line topology (see Section IV-A), and were individually tuned to compensate for transistor differences. The two amplifiers were combined for balanced amplifier operation through external commercial 3-dB quadrature couplers, and the measured results are shown in Fig. 12. Saturation and intermodulation distortion measurements were not made.

Series Line/Shunt Stub Matching: The integrated FET amplifier stages, whose characteristics were discussed in Section IV-A, were directly combined with dual microstrip 3-dB quadrature couplers of Lange design [13]. A photograph of this balanced FET amplifier is shown in Fig. 13. The individual stages, as mentioned earlier, employed devices of differing gain, power response, and transfer characteristics. A large differential transfer phase between

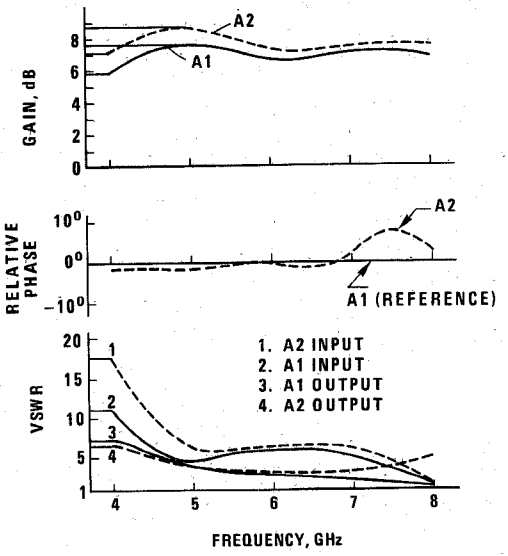


Fig. 11. Measured characteristics of a matched pair of MESFET amplifiers (circuits similar to Fig. 7).

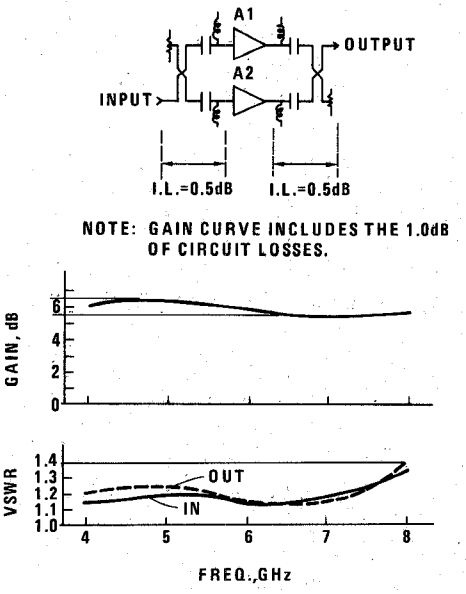


Fig. 12. Measured characteristics of matched amplifier pair of Fig. 11 in balanced configuration.

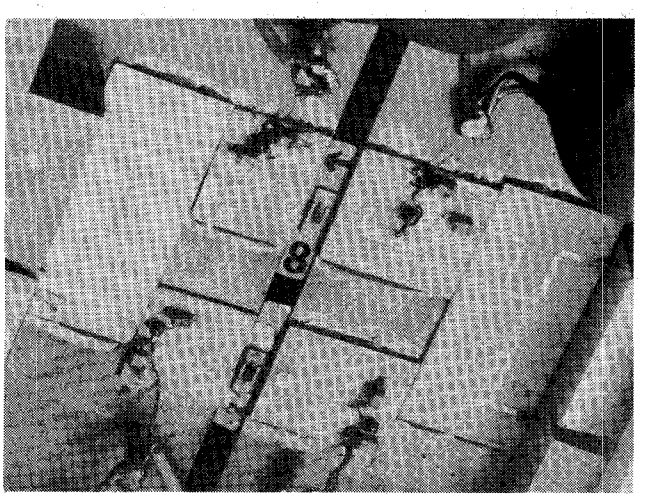


Fig. 13. Photograph of integrated balanced MESFET amplifier.

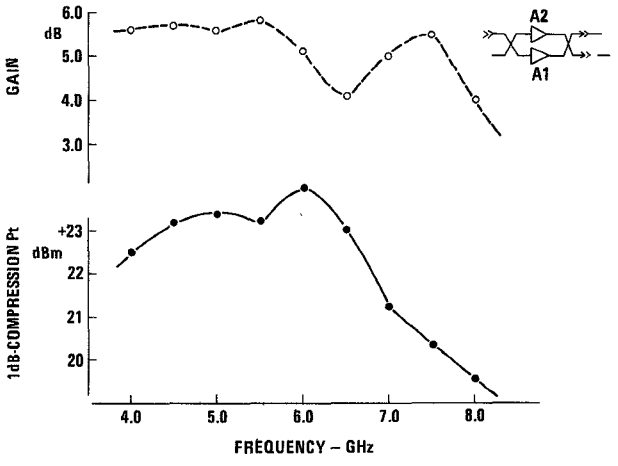


Fig. 14. Small-signal gain and output power at 1-dB gain compression for integrated balanced amplifier.

the two amplifiers was shown in Fig. 8. No attempts were made to alter the amplifier characteristics (phase response, etc.) discussed in Section IV-A before combining. Gain, power, and distortion measurements were taken. Fig. 14 gives plots of the measured gain and power compression response of the balanced amplifier. Over the 4.5–6.5-GHz band the 1-dB compression level is at an output power of 200 mW or greater. Improved gain and power response characteristics can, of course, be obtained by employing devices of a more similar nature and by selective tuning of the individual amplifiers. A third-order intermodulation level measured at 6 GHz was 40 dB below the output signal of +14 dBm. The corresponding intercept point is at approximately +35 dBm, about 7 dB higher than the worse of the two individual amplifiers, which agrees with Kurokawa's [12] estimate of 6–9 dB.

V. Conclusions

Octave bandwidth power MESFET amplifiers appear reasonably straightforward for power levels up to about ½ W with flat gain approaching GMAX at the upper end of the octave. Decade bandwidth from 1 to 10 GHz appears feasible with some sacrifice of overall gain.

In general, as power level increases, the attainable bandwidth decreases if unit cells are combined by paralleling at the chip, due to the parasitic attachment elements. Hence parasitic optimization eventually becomes imperative if bandwidth is to be maintained. The power level at which this occurs depends on the bandwidth needed. This is equivalent to "chip matching" commonly used in multicell bipolar power transistors. Further power addition through quadrature combination of amplifiers is desirable for VSWR reduction and intermodulation improvement.

Other areas for additional wide-band circuit work include the study of the perturbation of the device parameters under large-signal conditions so that the effect can be computed and the development of multioctave 3-dB quadrature directional couplers for microstrip application.

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